Bryan Lavin-Parmenter

Digital Hardware Engineer

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EXPERIENCE

Digital Hardware Engineering Intern — Qualcomm — June 2018 - September 2018

- Designed custom hardware IP using SystemVerilog for premium-tier mobile platform
  - Verified design with full UVM test suite including assertion-based, coverage-based, and randomized test generation in order to ensure design was functional on all edge cases
  - Used Synopsys Spyglass to capture clock domain crossing and DRC errors early in design process
  - Synthesized IP and performed verification to ensure design was synthesized correctly
- Developed custom verification software using Python to perform automated checks on tool-based RTL
  - Implemented memory mapping verification to automate error detection in address mappings
  - Created visualization tools to determine clock domain crossings and worst-case timing analysis
  - Worked with design engineers to ensure software outputs were correct and relevant to development

Software Development Engineering Intern — Amazon — June 2017 - September 2017

- Took ownership of summer internship software project through entire software development life cycle: analysis, planning, design, implementation, testing, and delivering results
- Developed health-detection application for automated detection and removal of faulty webservers
- Exceeded initial project goals resulting in a 93% reduction in time taken for removal of a faulty webserver

EDUCATION

University of California, Santa Barbara (UCSB)

- M.S. Electrical and Computer Engineering, Class of 2019
  - GPA: 3.63 / 4.00
- B.S. Electrical and Computer Engineering, Class of 2018
  - GPA: 3.38 / 4.00

PROFESSIONAL AND TECHNICAL SKILLS

- Internship experience and relevant coursework in RTL Design, Verification, and Synthesis
- Over 3 years experience and relevant coursework with SystemVerilog and UVM
- Over 5 years experience scripting in Python, C, and C++
- Experience using Python and machine learning toolkit for RTL Design Automation
- Knowledge of modern computer architecture including network-on-chip interconnect design
- Exposure to ASIC power analysis and static timing analysis
- Experience using Synopsys Spyglass and Design Compiler
- Exposure to machine learning for design test and verification
- Over 3 years experience with object-oriented design paradigms and design patterns
- Experience with FPGA embedded system design and development using Xilinx Vivado

ACTIVITIES

Graduate Teaching Assistant — UC Santa Barbara — September 2018 - June 2019

- ECE 10A: Instructed sophomore engineering students through basic circuit analysis and proctored labs
- ECE 5: Mentored freshman electrical engineering students through Arduino-based coursework. Managed 28 groups of 3+ students over 10 weeks to design and develop student-created Arduino projects.