Bryan Lavin-Parmenter

Digital ASIC Design & Implementation Engineer

blavin96@gmail.com
San Diego, CA
(916) 671 0541
linkedin.com/in/bryanlavinparmenter

EXPERIENCE

Qualcomm Technologies, Inc. | San Diego, CA

Sr. Digital Hardware Engineer | Qualcomm DDRPHY | 11/2021 - Present

- RTL Design Lead
  - Architected and implemented many designs including FIFOs, FSMs, datapaths, and debug features
  - Optimized logic blocks to increase maximum frequency by 50% in 3 years with minimal impact to power
  - Drove aggressive F/V plan optimizations leading to 10% digital power reduction in 1 year
  - Worked closely with standard-cell and technology teams to optimize cell selection for improved PPA
  - Drove initiatives to decrease LEF height by 5% through architectural updates and gate-level cell selection
  - Supervised the RTL design, integration, and verification efforts of multiple junior engineers
- DDRPHY Implementation Lead
  - Converted synthesis flow to physically-aware and improved standard cell PPA by 10% in one project
  - Brought forward recipe optimizations to improve design timing and decrease digital leakage by 5%
  - Utilized machine learning to further optimize synthesis recipe saving 2% in digital leakage and 1% in area
  - Responsible for constraint development, STA, and timing closure in front-end and back-end implementation
  - Served as the primary point-of-contact for front-end implementation within the mixed-signal organization
- DDRPHY Integration Lead
  - Accountable for end-to-end RTL execution, sign-off, and timely delivery of DDRPHY IP across multiple chips
  - Responsible for alignment and sign-off of all front-end tools including Lint, CDC, and Synthesis
  - Served as main point-of-contact across all teams in DDRPHY for design architecture, updates, and schedules
  - Managed and implemented many key initiatives to reduce RTL delivery time by multiple weeks per chip
  - Mentored three summer interns over a two-year period, resulting in a 100% return rate
- Awards
  - Won "best paper and presentation in digital design" at CadenceLIVE 2024 for DDRPHY implementation flow
  - Selected for "best poster" in digital front-end implementation at internal Qualcomm PPA conference
  - Awarded Qualcomm "Distinguished Solution" recognition for design to improve device reliability
  - Selected as "best digital design presentation" at Qualcomm internal conference for work on DDRPHY DFT

Digital Hardware Engineer | 07/2019 - 11/2021

- DDRPHY DFT Lead and Architect
  - Led DDRPHY DFT, owning scan connectivity, coverage analysis, pattern generation, and fault simulations
  - Achieved 3% higher stuck-at fault coverage over 2 years through design updates and DFT strategies
  - Implemented DFT clock architecture to improve DFT coverage with no impact to mission-mode performance
- DDRPHY Synthesis Lead
  - Performed DDRPHY synthesis in Design Compiler, owning netlist CLP, LEC, DFT, STA, ECO, and sign-off
  - Optimized logical synthesis recipe, cutting runtime 40% without compromising power, performance, or area
- RTL Designer
  - Engineered BIST modules and optimized test paths, decreasing test time and duty-cycle distortion
  - Tuned multi-GHz clocking architecture using gate-level swaps, cutting distortion, jitter, and delay by 10%+

Digital Hardware Engineer Intern | 06/2018 - 06/2018

EDUCATION

University of California, Santa Barbara

- M.S. Electrical and Computer Engineering, 2018 - 2019
- B.S. Electrical and Computer Engineering, 2014 - 2018
- 2018-2019 ECE Outstanding Teaching Assistant Award Winner

TECHINCAL SKILLS

RTL Design in SystemVerilog
Synthesis in Design Compiler and Genus
Static Timing Analysis in PrimeTime
CLP, LEC, and CECO in Conformal